ABSTRACT

A method and apparatus is described for the in-system programming of EEPROMs with configuration code for programmable logic devices such as FPGAs. The method and apparatus is suitable for use in larger systems where not all of the EEPROMs are located on the same circuit board. Multiple board-specific serial busses are provided, where each serial bus connects to EEPROMs of a particular circuit boards and to a common configuration point having selection apparatus and a header for coupling to configuration apparatus. The method includes the steps of setting the selection apparatus to designate a particular bus, erasing at least one EEPROM coupled to the serial bus, and writing programmable logic device configuration code through the serial bus to the EEPROM. Further claims include accessing the bus prior to writing any EEPROM to verify compatibility of a code file with the selected circuit board.